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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/628,562	07/29/2003	Bi-Yun Yeh	SUND 114CIP	4818

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RABIN & Berdo, PC
1101 14TH STREET, NW
SUITE 500
WASHINGTON, DC 20005

EXAMINER	
RAHMAN, FAHMIDA	
ART UNIT	**PAPER NUMBER**
2116	

DATE MAILED: 12/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/628,562	YEH ET AL.	
	Examiner	Art Unit	
	Fahmida Rahman	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31* is/are rejected.

7)☒ Claim(s) *2,14 and 16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-31 are pending.

Priority

Acknowledgment is made of applicant's claim for foreign priority based on an application filed in Taiwan on 6/14/1999. It is noted, however, that applicant has not filed a certified copy of the application 88109868 as required by 35 U.S.C. 119(b).

Information Disclosure Statement

The information disclosure statement (IDS) submitted on 7/29/2003 is considered by the examiner. However, applicant should submit a PTO-1449 including the lists of patents and non-patent documents. The submitted form is not a replacement for 1449, since it does not have any space to put initial for examiner. Accordingly, the submitted form is not attached in the file.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., In re Berg, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); In re Goodman, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); In re Longi, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); In re Van Ornum, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); In re Vogel, 422

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1-31 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-33 of U.S. Patent No.6691224. Although the conflicting claims are not identical, they are not patentably distinct from each other because both the pending application and the patent disclose a method for accessing initialization data for starting a central processing unit in a computer system by starting up a north bridge chip, sending request to south bridge chip by north bridge chip for initialization data and receiving initialization data by north bridge. Both of the application and patent comprise activating South bridge chip by power supplier/controller, SIP and ID as initialization data, a boot ROM storing initialization data for performing the access of initialization data for starting CPU in the computer system.

Claim Objections

Claims 2, 14, 16 are objected to because of the following informalities:

The unnecessary character "[?]" in line 2 of claim 2 should be removed.

"1 2" should be written as "12" in claims 14 and 16.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 7, 9, 12, 15-17, 20, 22, 27 are rejected under 35 U.S.C. 102(e) as being anticipated by Klein (US Patent 6216224).

For claim 7, Klein teaches the following limitations:

A method for accessing initialization data of a central processor unit (lines 55-57 of column 3) **by a South-bridge chip** (110) **in a computer system** (Fig 1) **comprising:**

- **accessing initialization data** (102) **by said south-bridge chip (110);**
- **and sending initialization data by said south-bridge chip** (Fig 1 is showing that ROM initialization data is transmitted from 104 to 116 through South Bridge 110).

For claim 9, 104 is the boot ROM, since it contains BIOS.

For claim 12, Klein teaches the following limitations:

A method for accessing initialization data (102 in Fig 1) **for starting a central processor unit** (lines 55-57 of column 3; lines 5-10 of column 1) **in a computer system** (Fig 1) **comprising:**

- **requesting the initialization data by a north bridge chip from a south bridge chip** (lines 25-30 of column 3 mention that the system controller 114 transfers ROM data 102 to RAM 118. Thus, the North Bridge 114 requests for initialization data 102 through South Bridge 110);
- **accessing the initialization data stored in a non-volatile memory by the south bridge chip** (Fig 1);
- **and activating the central processor unit based on the initialization data received by the north-bridge chip from the south bridge chip** (lines 1-20 of column 2).

For claim 15, 104 is the ROM containing BIOS.

For claim 16, the mentioned steps are required for transferring initialization data from non-volatile memory to system memory through South Bridge under the driving of North Bridge.

For claim 17, note lines 1-17 of column 2.

For claim 20, Klein teaches the following limitations:

a system **for accessing initialization data** (102 in Fig 1) **for starting a central processor unit** (lines 55-57 of column 3; lines 5-10 of column 1), **the system comprising:**

- **a north bridge chip** (114 is a North Bridge because it is closer to CPU, connected to system memory and bridges CPU-PCI bus) **in direct communication with a south bridge chip** (110 is a South Bridge chip because it bridges PCI-ISA) **and the central processor unit** (106);
- **and a non-volatile memory subsystem** (104) **in direct communication with the south bridge chip storing the initialization data** (102);
- **wherein upon receiving a request from the north bridge chip for obtaining the initialization data** (lines 27 of column 3 mention that the system controller is to transfer the ROM data to RAM. Thus, the North Bridge does the request to obtain ROM data from 104), **the initialization data is accessed by the south bridge chip** (Fig 1) **and forwarded to the north bridge chip** (lines 1-5 of column 2) **for activating the central processor unit** (lines 1-20 of column 2).

For claim 22, 104 is the ROM containing BIOS.

For claim 27, lines 1-17 of column 2 mention that CPU reads initialization data.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-6, 8, 10-11, 13-14, 19, 21, 25-26, 28-29 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admission of prior art, in view of Klein (US Patent 6216224).

For claim 1, applicant admits that the following limitations exist in prior art:

A method for accessing initialization data for starting a central processor unit in a computer system (Fig 1 and 2 show that the serial PROM 200 is storing initialization data for starting a central processing unit 208 in a computer system of Fig 1) **comprising:**

- **starting up a north-bridge chip** (line 20 of page 3);
- **requesting said initialization data by said north bridge chip** (lines 20-22 of page 3);
- **receiving said initialization data by said north-bridge chip** (lines 21-22 of page 3).

However, the applicant's admission of prior art does not teach the following limitations:

- **requesting initialization data from a south bridge chip.**

Klein teaches a system where BIOS and initialization data (102) is in a memory 104 connected to South Bridge 110 (Line 28 of column 4 mention that 110 is a PCI-ISA bridge, which is the South Bridge). The memory 104 connected to South Bridge 110 is storing both BIOS and initialization routines (lines 28-33 of column 1 mention that the firmware routines include BIOS and other initialization routines.

It would have been obvious to one ordinary skill in the art to combine the teachings of Klein and applicant's admission of prior art. One ordinary skill in the art would have been motivated to request initialization data of CPU from a South Bridge chip as disclosed in Klein, since it would make the system compact as only one shared non-volatile memory for BIOS and initialization data is required, which is accessed by CPU through South Bridge.

For claims 2, 3, 8, lines 23-24 of page 2 of applicant's disclosure mention that the initialization data may include SIP data used in AMD CPUs.

For claim 4, note lines 19-21 of [0007] of page 3 of applicant's disclosure, which mention that the South Bridge is powered and starts up the North Bridge.

For claim 5, requesting includes sending a signal from north bridge chip (114) to South bridge chip (104).

For claim 6, lines 22-24 of [0007] of page 3 of applicant's disclosure mention that the CPU sets initial value using initialization data sent by North Bridge and operates normally. Thus, the method further comprises sending said initialization data to the central processor unit of said computer system for starting up the central processor unit.

For claim 10, note lines 19-21 of [0007] of page 3 of applicant's disclosure, which mention that the South Bridge is powered and starts up the North Bridge.

However, applicant's admission of prior art does not mention about accessing initialization data by South Bridge after the North Bridge sends request for initialization data.

Klein teaches that the North Bridge 110 is reading initialization data from South Bridge 104. Thus, the North Bridge passes associated signals to South Bridge.

It would have been obvious for an ordinary skill in the art to combine the teachings of applicant's admission of prior art and Klein. One ordinary skill in the art would have been motivated to send request signal from North Bridge to South Bridge, since North Bridge is closer to CPU and coupled to system memory, where the initialization routines would be transferred. Thus, the North Bridge has to send the signals associated with reading the data to South Bridge.

For claim 11, note lines 1-15 of claim 2.

For claim 13, note lines 19-21 of [0007] of page 3 of applicant's disclosure, which mention that the South Bridge is powered and starts up the North Bridge.

For claim 14, note Fig 1 of applicant's disclosure.

For claims 18, 23 and 30, Klein mentions that the address counter preloads an initial address, which is the highest address for ROM data that is transferred from ROM to RAM in lines 30-35 of column 5. Thus, the ROM data contains an initialization ID.

For claim 19, lines 23-24 of page 2 of applicant's disclosure mention that the initialization data may include SIP data used in AMD CPUs.

For claim 21, Fig 1 of applicant's disclosure show that South Bridge is connected to power supply controller.

For claim 24, Klein mentions that the address counter preloads an initial address, which is the highest address for ROM data that is transferred from ROM to RAM and the initial address may be provided by hardwiring in lines 30-50 of column 5. Thus, ROM includes a predetermined location for storing initialization data. Lines 50-55 of column 1 mention that after the CPU initialization is executed, it can be discarded and the RAM contains

remaining BIOS. Thus, the initialization routines and BIOS have to be stored in separate area because they are separate routines.

For claim 25, lines 23-24 of page 2 of applicant's disclosure mention that the initialization data may include SIP data used in AMD CPUs.

For claim 26, Klein is retrieving the initialization data by the south bridge chip; and sending the initialization data to the north bridge chip.

However the south bridge chip of Klein does not include means for: activating the north bridge chip. Applicant's admission of prior art activates North Bridge by South Bridge.

It would have been obvious to one ordinary skill in the art to have combined the teachings of applicant's admission of prior art and Klein. One ordinary skill in the art would have been motivated to activate the North Bridge by South Bridge as disclosed in applicant's admission of prior art, since South Bridge contains the initialization data, which should be started before other components.

For claim 28, applicant's admission of prior art teaches the following limitations:

a method for accessing initialization data for starting a central processor unit in a computer system (Fig 1 and 2 show that the serial PROM 200 is storing initialization

data for starting a central processing unit 208 in a computer system of Fig 1), **the method comprising:**

- **activating a south bridge chip by a power supplier controller** (lines 17-18 of [0007] of page 3 mention that the South Bridge is powered when the system is powered on. Fig 1 shows that the South Bridge is connected to power supply controller. Thus, the South Bridge chip is activated by by the power supply controller);
- **activating a north bridge chip by the activated south bridge chip** (lines 19-22 of [0007] of page 3 mention that the South Bridge sends a signal to start North bridge); requesting to access the initialization data (lines 20-23 of [0007] of page 3 mention that the North bridge sends request to access initialization data);
- **accessing the initialization data stored in a non-volatile memory** (200 of Fig 2 contains initialization data, which is a Non-volatile memory);
- **sending the initialization data to the north bridge chip** (Lines 21-23 of [0007] of page 3 mention that the North bridge receives initialization data);
- **sending an initialization signal to the central processor unit by the north bridge chip upon receiving the initialization data** (lines 20-25 of [0007] of page 3 mention that CPU uses initialization data sent by North Bridge);
- **and activating the central processor unit by the initialization signal** (lines 23-25 of [0007] of page 3 mention that the CPU operates normally after setting initial values).

Applicant's admission of Prior Art does not teach the following limitations of claim 28:

- Requesting South Bridge chip for initialization data
- Accessing initialization data by South Bridge
- Sending initialization data by South Bridge

The system of Klein teaches that the non-volatile ROM containing initialization data 102 is transferred to RAM under the driving of North Bridge through South Bridge 110. For that, the usual procedures have to include requesting for initialization data through South Bridge, accessing initialization data by South Bridge and sending initialization data by South Bridge.

It would have been obvious to one ordinary skill in the art to combine the teachings of Klein and applicant's admission of prior art. One ordinary skill in the art would have been motivated to request initialization data of CPU from a South Bridge chip as disclosed in Klein, since it would make the system compact as only one shared non-volatile memory for BIOS and initialization data is required, which is accessed by CPU through South Bridge.

For claim 29, 104 of Klein is a non-volatile memory containing BIOS.

For claims 31, lines 23-24 of page 2 of applicant's disclosure mention that the initialization data may include SIP data used in AMD CPUs.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fahmida Rahman whose telephone number is 571-272-8159. The examiner can normally be reached on Monday through Friday 8:30 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on 571-272-3670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Fahmida Rahman
Examiner
Art Unit 2116

LYNNE H. BROWNE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100